National Semiconductor

November 1999

ADC10154/ADC10158
10-Bit Plus Sign 4 µs ADCs with 4- or 8-Channel MUX, Track/Hold and Reference

General Description

The ADC10154 and ADC10158 are CMOS 10-bit plus sign successive approximation A/D converters with versatile analog input multiplexers, track/hold function and a 2.5V band-gap reference. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The input track/hold is implemented using a capacitive array and sampled-data comparator.

Resolution can be programmed to be 8-bit, 8-bit plus sign, 10-bit or 10-bit plus sign. Lower-resolution conversions can be performed faster.

The variable resolution output data word is read in two bytes, and can be formatted left justified or right justified, high byte first.

Applications

- Process control
- Instrumentation
- Test equipment

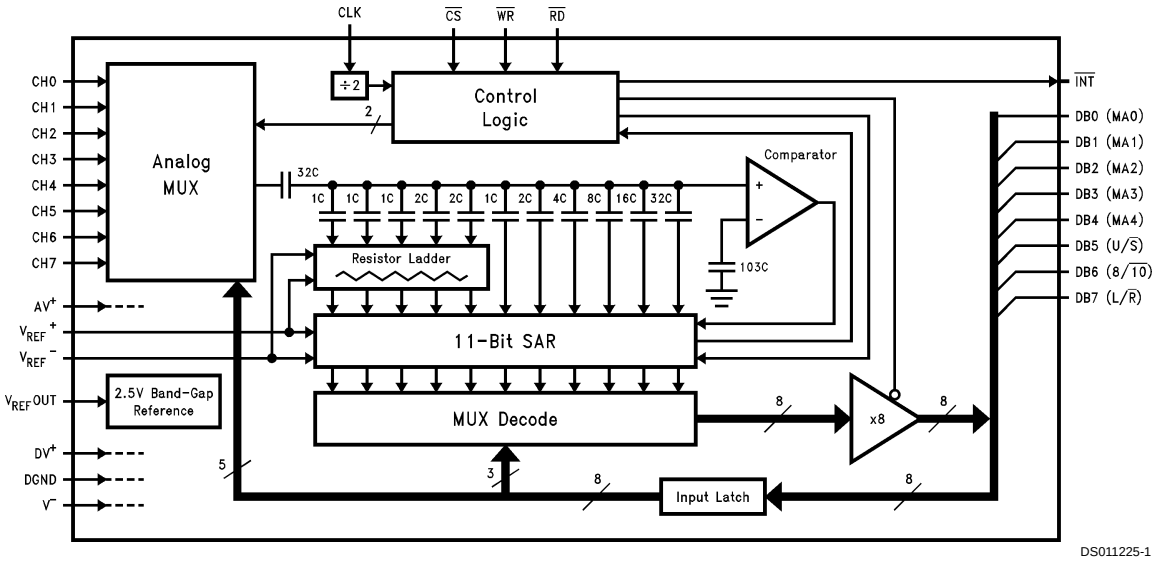
Features

- 4- or 8- channel configurable multiplexer
- Analog input track/hold function
- 0V to 5V analog input range with single +5V power supply
- −5V to +5V analog input voltage range with ±5V supplies
- Fully tested in unipolar (single +5V supply) and bipolar (dual ±5V supplies) operation
- Programmable resolution/speed and output data format
- Ratiometric or Absolute voltage reference operation
- No zero or full scale adjustment required
- No missing codes over temperature
- Easy microprocessor interface

Key Specifications

Resolution	10-bit plus sign
Integral linearity error	±1 LSB (max)
Unipolar power dissipation	33 mW (max)
Conversion time (10-bit + sign)	4.4 µs (max)
Conversion time (8-bit)	3.2 µs (max)
Sampling rate (10-bit + sign)	166 kHz
Sampling rate (8-bit)	207 kHz
Band-gap reference	2.5V ±2.0% (max)

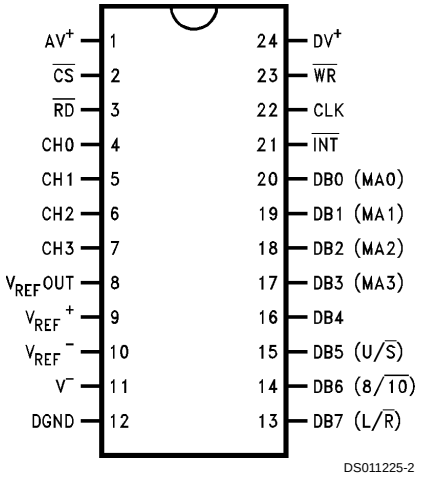
ADC10158 Simplified Block Diagram



© 2001 National Semiconductor Corporation

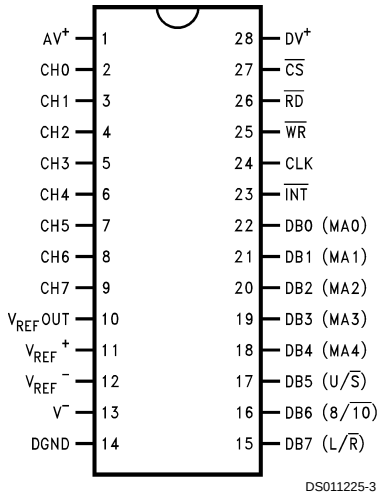
Connection Diagrams

Dual-in-Line and SO Packages



Top View
Order Number ADC10154
NS Package Number M24B

Dual-in-Line and SO Packages



Top View
Order Number ADC10158
NS Package Numbers
M28B or N28B

Pin Descriptions

AV^+ This is the positive analog supply. This pin should be bypassed with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor to the system analog ground.

DV^+ This is the positive digital supply. This supply pin also needs to be bypassed with 0.1 µF ceramic and 10 µF tantalum capacitors to the system digital ground. AV^+ and DV^+ should be bypassed separately and tied to same power supply.

DGND This is the digital ground. All logic levels are referred to this ground.

V^- This is the negative analog supply. For unipolar operation this pin may be tied to the system analog ground or to a negative supply source. It should not go above DGND by more than 50 mV. When bipolar operation is required, the voltage on this pin will limit the analog input's negative voltage level. In bipolar operation this supply pin needs to be bypassed with 0.1 µF ceramic and 10 µF tantalum capacitors to the system analog ground.

V_{REF}^+, V_{REF}^- These are the positive and negative reference inputs. The voltage difference between V_{REF}^+ and V_{REF}^- will set the analog input voltage span.

V_{REF}Out This is the internal band-gap voltage reference output. For proper operation of the voltage reference, this pin needs to be bypassed with a 330 µF tantalum or electrolytic capacitor.

$\overline{CS}$ This is the chip select input. When a logic low is applied to this pin the $\overline{WR}$ and $\overline{RD}$ pins are enabled.

$\overline{RD}$ This is the read control input. When a logic low is applied to this pin the digital outputs are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ This is the write control input. The rising edge of the signal applied to this pin selects the multiplexer channel and initiates a conversion.

$\overline{INT}$ This is the interrupt output. A logic low at this output indicates the completion of a conversion.

CLK This is the clock input. The clock frequency directly controls the duration of the conversion time (for example, in the 10-bit bipolar mode $t_C = 22/f_{CLK}$) and the acquisition time ($t_A = 6/f_{CLK}$).

DB0(MA0) –DB7 (L/$\overline{R}$) These are the digital data inputs/outputs. DB0 is the least significant bit of the digital output word; DB7 is the most significant bit in the digital output word (see the Output Data Configuration table). MA0 through MA4 are the digital inputs for the multiplexer channel selection (see the Multiplexer Addressing tables). U/$\overline{S}$ (Unsigned/Signed), 8/$\overline{10}$, (8/10-bit resolution) and L/$\overline{R}$ (Left/Right justification) are the digital input bits that set the A/D's output word format and resolution (see the Output Data Configuration table). The conversion time is modified by the chosen resolution (see Electrical AC Characteristics table). The lower the resolution, the faster the conversion will be.

CH0–CH7 These are the analog input multiplexer channels. They can be configured as single-ended inputs, differential input pairs, or pseudo-differential inputs (see the Multiplexer Addressing tables for the input polarity assignments).

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage ($V^+ = AV^+ = DV^+$)	6.5V
Negative Supply Voltage (V^-)	−6.5V
Total Supply Voltage ($V^+ - V^-$)	13V
Total Reference Voltage ($V_{REF}^+ - V_{REF}^-$)	6.6V
Voltage at Inputs and Outputs	$V^- - 0.3V$ to $V^+ + 0.3V$
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Package Dissipation at $T_A = 25^\circ C$ (Note 5)	500 mW
ESD Susceptibility (Note 6)	2000V
Soldering Information	
N Packages (10 Sec)	260˚C
J Packages (10 Sec)	300˚C
SO Package (Note 7):	
Vapor Phase (60 Sec)	215˚C
Infrared (15 Sec)	220˚C
Storage Temperature	
Ceramic DIP Packages	−65˚C to +150˚C
Plastic DIP and SO Packages	−40˚C to +150˚C

Operating Ratings (Notes 2, 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC10154CIWM, ADC10158CIN, ADC10158CIWM	$-40^\circ C \le T_A \le +85^\circ C$
Positive Supply Voltage ($V^+ = AV^+ = DV^+$)	4.5 V_{DC} to 5.5 V_{DC}
Unipolar Negative Supply Voltage (V^-)	DGND
Bipolar Negative Supply Voltage (V^-)	−4.5V to −5.5V
$V^+ - V^-$	11V
V_{REF}^+	$AV^+ + 0.05\ V_{DC}$ to $V^- - 0.05\ V_{DC}$
V_{REF}^-	$AV^+ + 0.05\ V_{DC}$ to $V^- - 0.05\ V_{DC}$
V_{REF} ($V_{REF}^+ - V_{REF}^-$)	0.5 V_{DC} to V^+

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 5.000\ V_{DC}$, $V_{REF}^- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$. (Notes 8, 9, 12)

Symbol	Parameter	Conditions	Typical (Note 10)	CIN and CIWM Suffixes Limits (Note 11)	Units (Limit)
UNIPOLAR CONVERTER AND MULTIPLEXER STATIC CHARACTERISTICS					
	Resolution			**10 + Sign**	Bits
	Unipolar Integral Linearity Error	$V_{REF}^+ = 2.5V$	±0.5		LSB
		$V_{REF}^+ = 5.0V$		**±1**	LSB (Max)
	Unipolar Full-Scale Error	$V_{REF}^+ = 2.5V$	±0.5		LSB
		$V_{REF}^+ = 5.0V$		**±1.5**	LSB (Max)
	Unipolar Offset Error	$V_{REF}^+ = 2.5V$	±1		LSB
		$V_{REF}^+ = 5.0V$		**±2**	LSB (Max)
	Unipolar Total Unadjusted Error (Note 13)	$V_{REF}^+ = 2.5V$	±1.5		LSB
		$V_{REF}^+ = 5.0V$		**±2.5**	LSB (Max)
	Unipolar Power Supply Sensitivity	$V^+ = +5V$ ±10% $V_{REF}^+ = 4.5V$			
	Offset Error		±0.25	**±1**	LSB (Max)
	Full-Scale Error		±0.25	**±1**	LSB (Max)
	Integral Linearity Error		±0.25		LSB
BIPOLAR CONVERTER AND MULTIPLEXER STATIC CHARACTERISTICS					
	Resolution			**10 + Sign**	Bits
	Bipolar Integral Linearity Error	$V_{REF}^+ = 5.0V$		**±1**	LSB (Max)
	Bipolar Full-Scale Error	$V_{REF}^+ = 5.0V$		**±1.25**	LSB (Max)

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 5.000\ V_{DC}$, $V_{REF}^- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$. (Notes 8, 9, 12)

Symbol	Parameter	Conditions	Typical (Note 10)	CIN and CIWM Suffixes Limits (Note 11)	Units (Limit)
BIPOLAR CONVERTER AND MULTIPLEXER STATIC CHARACTERISTICS					
	Bipolar Negative Full-Scale Error with Positive-Full Scale Adjusted	$V_{REF}^+ = 5.0V$		**±1.25**	LSB (Max)
	Bipolar Offset Error	$V_{REF}^+ = 5.0V$		**±2.5**	LSB (Max)
	Bipolar Total Unadjusted Error (Note 13)	$V_{REF}^+ = 5.0V$		**±3**	LSB (Max)
	Bipolar Power Supply Sensitivity				
	Offset Error	$V^+ = +5V \pm 10\%$	±0.5	**±2.5**	LSB (Max)
	Full-Scale Error	$V_{REF}^+ = 4.5V$	±0.5	**±1.5**	LSB (Max)
	Integral Linearity Error		±0.25		LSB
	Offset Error	$V^- = -5V \pm 10\%$	±0.25	**±0.75**	LSB (Max)
	Full-Scale Error	$V_{REF}^+ = 4.5V$	±0.25	**±0.75**	LSB (Max)
	Integral Linearity Error		±0.25		LSB
UNIPOLAR AND BIPOLAR CONVERTER AND MULTIPLEXER STATIC CHARACTERISTICS					
	Missing Codes			**0**	
	DC Common Mode Error (Note 14)	$V_{IN}^+ = V_{IN}^-$ = V_{IN} where			
	Bipolar	$+5.0V \geq V_{IN} \geq -5.0V$	±0.25	**±0.75**	LSB (Max)
	Unipolar	$+5.0V \geq V_{IN} \geq 0V$	±0.25	**±0.5**	LSB (Max)
R_{REF}	Reference Input Resistance		7	**4.5** **9.5**	kΩ (Max) kΩ (Max)
C_{REF}	Reference Input Capacitance		70		pF
V_{AI}	Analog Input Voltage			**(V^++0.05)** **(V^-−0.05)**	V (Max) V (Min)
C_{AI}	Analog Input Capacitance		30		pF
	Off Channel Leakage Current (Note 15)	On Channel = 5V Off Channel = 0V	−400	**−1000**	nA (Max)
		On Channel = 0V Off Channel = 5V	400	**1000**	nA (Max)

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 5.000\ V_{DC}$, $V_{REF}^- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$. (Notes 8, 9, 12)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
DYNAMIC CONVERTER AND MULTIPLEXER CHARACTERISTICS					
S/(N+D)	Unipolar Signal-to-Noise+ Distortion Ratio	$f_{IN} = 10$ kHz, $V_{IN} = 4.85\ V_{p-p}$	60		dB
		$f_{IN} = 150$ kHz, $V_{IN} = 4.85\ V_{p-p}$	58		dB
S/(N+D)	Bipolar Signal-to-Noise+ Distortion Ratio	$f_{IN} = 10$ kHz, $V_{IN} = \pm 4.85V$	60		dB
		$f_{IN} = 150$ kHz, $V_{IN} = \pm 4.85V$	58		dB

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 5.000\ V_{DC}$, $V_{REF}^- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$. (Notes 8, 9, 12)

Symbol	Parameter		Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
DYNAMIC CONVERTER AND MULTIPLEXER CHARACTERISTICS						
	−3 dB Unipolar Full Power Bandwidth		$V_{IN} = 4.85\ V_{p-p}$	200		kHz
	−3 dB Bipolar Full Power Bandwidth		$V_{IN} = \pm 4.85V$	200		kHz
REFERENCE CHARACTERISTICS (Unipolar Operation $V^- = GND$ Only)						
VREFOut	Reference Output Voltage			2.5 ±1%	**2.5 ± 2%**	V (Max)
$\Delta V_{REF}/\Delta t$	VREFOut Temperature Coefficient			40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Load Regulation	Sourcing	$0\ mA \le I_L \le +4\ mA$	0.003	**0.1**	%/mA (Max)
		Sinking	$0\ mA \ge I_L \ge -1\ mA$	0.2	**0.6**	%/mA (Max)
	Line Regulation		$4.5V \le V^+ \le 5.5V$	0.5	**6**	mV (Max)
I_{SC}	Short Circuit Current		VREFOut = 0V	14	**25**	mA (Max)
$\Delta V_{REF}/\Delta t$	Long-Term Stability			200		ppm/1 kHr
t_{SU}	Start-Up Time		$C_L = 330\ \mu F$	20		ms
DIGITAL AND DC CHARACTERISTICS						
$V_{IN(1)}$	Logical “1” Input Voltage		$V^+ = 5.5V$		**2.0**	V (Min)
$V_{IN(0)}$	Logical “0” Input Voltage		$V^+ = 4.5V$		**0.8**	V (Max)
$I_{IN(1)}$	Logical “1” Input Current		$V_{IN} = 5.0V$	0.005	**2.5**	µA (Max)
$I_{IN(0)}$	Logical “0” Input Current		$V_{IN} = 0V$	−0.005	**−2.5**	µA (Max)
$V_{OUT(1)}$	Logical “1” Output Voltage		$V^+ = 4.5V$:			
			$I_{OUT} = -360\ \mu A$		**2.4**	V (Min)
			$I_{OUT} = -10\ \mu A$		**4.25**	V (Min)
$V_{OUT(0)}$	Logical “0” Output Voltage		$V^+ = 4.5V$, $I_{OUT} = 1.6\ mA$		**0.4**	V (Max)
I_{OUT}	TRI-STATE Output Current		$V_{OUT} = 0V$	−0.01	**−3**	µA (Max)
			$V_{OUT} = 5V$	0.01	**3**	µA (Max)
$+I_{SC}$	Output Short Circuit Source Current		$V_{OUT} = 0V$	−40	**−10**	mA (Min)
$-I_{SC}$	Output Short Circuit Sink Current		$V_{OUT} = DV^+$	30	**10**	mA (Min)
DI+	Digital Supply Current		$\overline{CS}$ = HIGH	0.75	**2**	mA (Max)
			$\overline{CS}$ = HIGH, $f_{CLK} = 0$ Hz	0.15		mA (Max)
AI^+	Analog Supply Current		$\overline{CS}$ = HIGH	3	**4.5**	mA (Max)
			$\overline{CS}$ = HIGH, $f_{CLK} = 0$ Hz	3		mA (Max)
I^-	Negative Supply Current		$\overline{CS}$ = HIGH	3.5	**4.5**	mA (Max)
			$\overline{CS}$ = HIGH, $f_{CLK} = 0$ Hz	3.5		mA (Max)
I_{REF}	Reference Input Current		$V_{REF}^+ = 5V$	0.7	**1.1**	mA (Max)

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 5.000\ V_{DC}$, $V_{REF}^- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$. (Note 16)

Symbol	Parameter		Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
AC CHARACTERISTICS						
f_{CLK}	Clock Frequency			8	**5.0**	MHz (Max)
				10		kHz (Min)
	Clock Duty Cycle				**20**	% (Min)
					80	% (Max)
t_C	Conversion Time	8-Bit Unipolar Mode			**16**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**3.2**	µs (Max)
		8-Bit Bipolar Mode			**18**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**3.6**	µs (Max)
		10-Bit Unipolar Mode			**20**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**4.0**	µs (Max)
		10-Bit Bipolar Mode			**22**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**4.4**	µs (Max)
t_A	Acquisition Time				**6**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**1.2**	µs
t_{CR}	Delay between Falling Edge of $\overline{CS}$ and Falling Edge of $\overline{RD}$			0	**5**	ns (Min)
t_{RC}	Delay betwee Rising Edge $\overline{RD}$ and Rising Edge of $\overline{CS}$			0	**5**	ns (Min)
t_{CW}	Delay between Falling Edge of $\overline{CS}$ and Falling Edge of $\overline{WR}$			0	**5**	ns (Min)
t_{WC}	Delay between Rising Edge of $\overline{WR}$ and Rising Edge of $\overline{CS}$			0	**5**	ns (Min)
t_{RW}	Delay between Falling Edge of $\overline{RD}$ and Falling Edge of $\overline{WR}$			0	**5**	ns (Min)
$t_{W(\overline{WR})}$	$\overline{WR}$ Pulse Width			25	**50**	ns (Min)
t_{WS}	$\overline{WR}$ High to CLK÷2 Low Set-Up Time				**5**	ns (Max)
t_{DS}	Data Set-Up Time			6	**15**	ns (Max)
t_{DH}	Data Hold Time			0	**5**	ns (Max)
$t_{\overline{WR}}$	Delay from Rising Edge of $\overline{WR}$ to Rising Edge $\overline{RD}$			0	**5**	ns (Min)
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)		$C_L = 100$ pF	25	**45**	ns (Max)
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of INT		$C_L = 100$ pF	25	**40**	ns (Max)
$t_{\overline{INTL}}$	Delay from Falling Edge of CLK÷2 to Falling Edge of $\overline{INT}$			40		ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)		$C_L = 10$ pF, $R_L = 1\ k\Omega$	20	**35**	ns (Max)
t_{RR}	Delay between Successive $\overline{RD}$ Pulses			25	**50**	ns (Min)
t_P	Delay between Last Rising Edge of $\overline{RD}$ and the Next Falling Edge of $\overline{WR}$			20	**50**	ns (Min)
C_{IN}	Capacitance of Logic Inputs			5		pF
C_{OUT}	Capacitance of Logic Outputs			5		pF

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

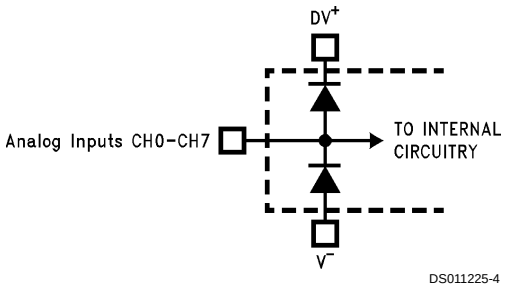
Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < V^-$ or $V_{IN} > AV^+$ or DV^+), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 150˚C. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow: ADC10154 with BIN and CIN suffixes 65˚C/W, ADC10154 with BIJ, CIJ and CMJ suffixes 49˚C/W, ADC10154 with BIWM and CIWM suffixes 72˚C/W, ADC10158 with BIN and CIN suffixes 59˚C/W, ADC10158 with BIJ, CIJ, and CMJ suffixes 46˚C/W, ADC10158 with BIWM and CIWM suffixes 68˚C/W.

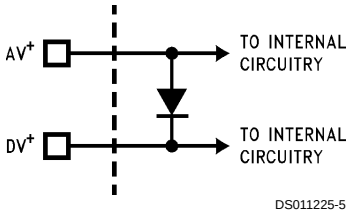
Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post-1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 8: Two on-chip diodes are tied to each analog input as shown below. They will forward-conduct for analog input voltages one diode drop below V^- supply or one diode drop greater than V^+ supply. Be careful during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors for analog inputs near full-scale. The specification allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. This means that if AV^+ and DV^+ are minimum (4.5 V_{DC}) and V^- is a maximum (−4.5 V_{DC}) full scale must be ≤ ±4.55 V_{DC}.



Note 9: A diode exists between AV^+ and DV^+ as shown below.



To guarantee accuracy, it is required that the AV^+ and DV^+ be connected together to a power supply with separate bypass filter at each V^+ pin.

Note 10: Typicals are at $T_J = T_A$ = 25˚C and represent most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: One LSB is referenced to 10 bits of resolution.

Note 13: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 14: For DC Common Mode Error the only specification that is measured is offset error.

Note 15: Channel leakage current is measured after the channel selection.

Note 16: All the timing specifications are tested at the TTL logic levels, V_{IL} = 0.8V for a falling edge and V_{IH} = 2.0V for a rising.

Electrical Characteristics (Continued)

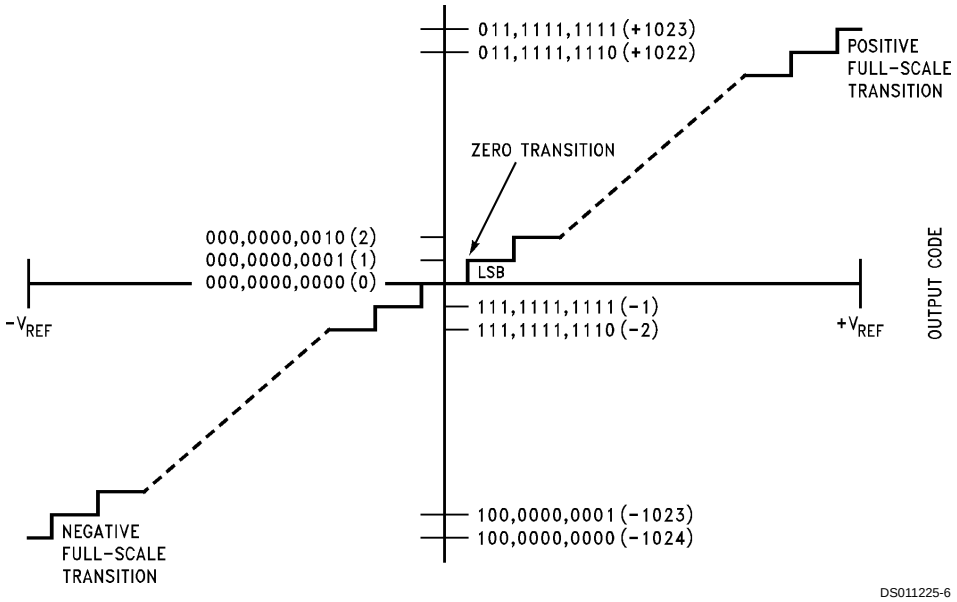


FIGURE 1. Transfer Characteristic

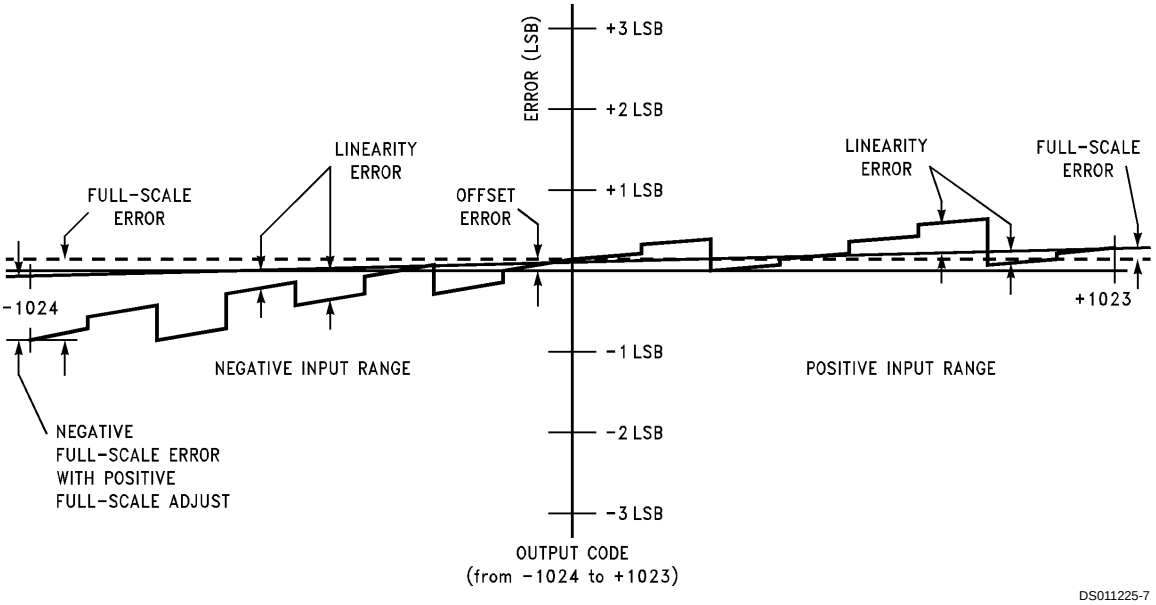


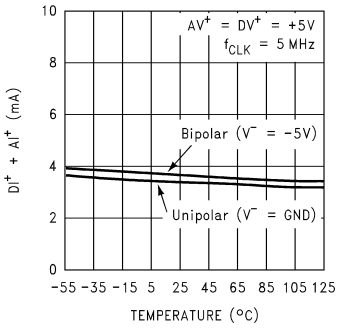
FIGURE 2. Simplified Error Curve vs Output Code

Ordering Information

Industrial −40˚C ≤ T_A ≤ 85˚C	Package
ADC10154CIWM	M24B
ADC10158CIN	N28B
ADC10158CIWM	M28B

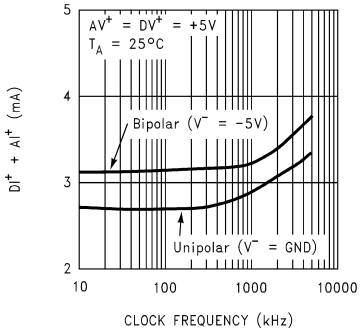
Typical Converter Performance Characteristics

Total Positive Supply Current ($DI^+ + AI^+$) vs Temperature



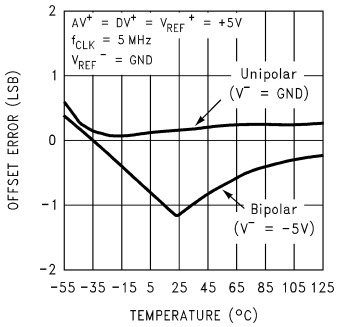
DS011225-27

Total Positive Power Supply Current ($DI^+ + AI^+$) vs Clock Frequency



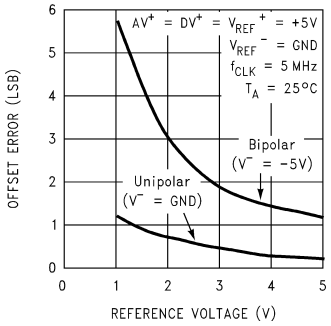
DS011225-28

Offset Error vs Temperature



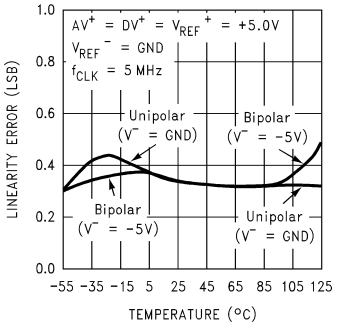
DS011225-29

Offset Error vs Reference Voltage



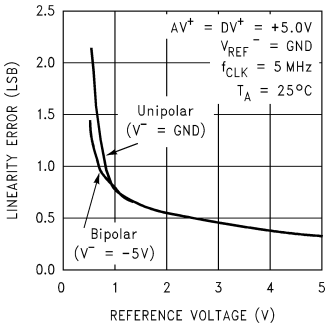
DS011225-30

Linearity Error vs Temperature



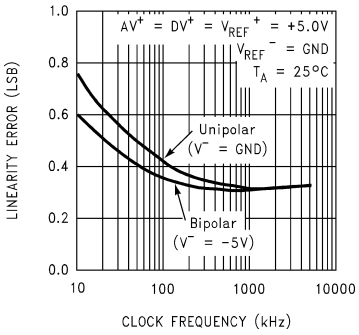
DS011225-31

Linearity Error vs Reference Voltage



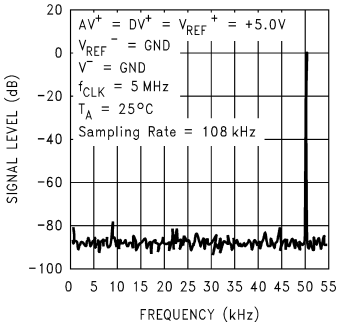
DS011225-32

Linearity Error vs Clock Frequency



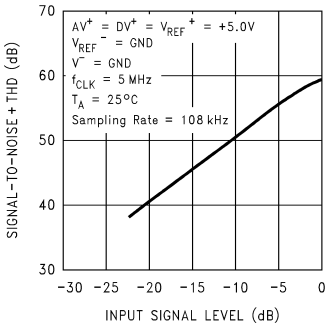
DS011225-33

Spectral Response with 50 kHz Sine Wave



DS011225-34

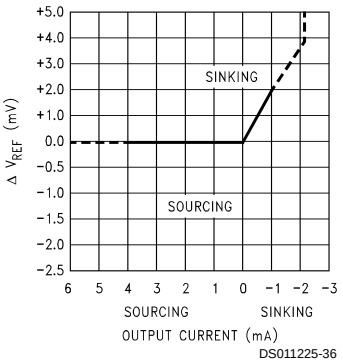
10-Bit Unsigned Signal-to-Noise + THD Ratio vs Input Signal Level



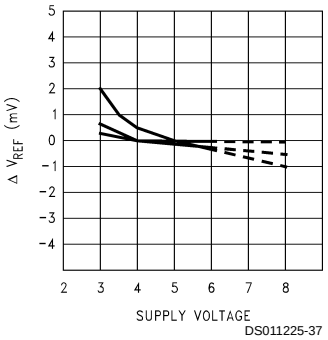
DS011225-35

Typical Reference Performance Characteristics

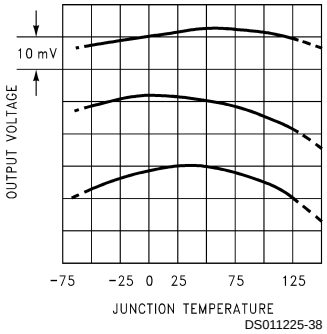
Load Regulation



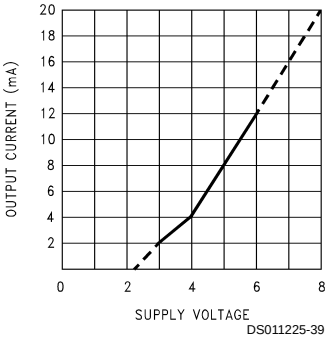
Line Regulation (3 Typical Parts)



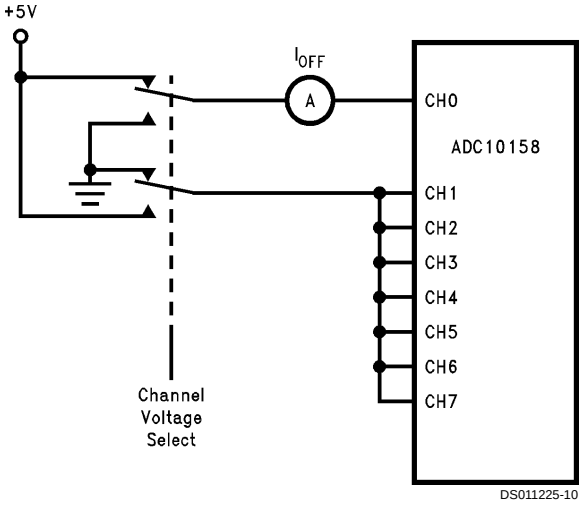
Output Drift vs Temperature (3 Typical Parts)



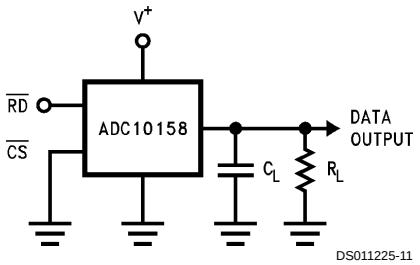
Available Output Current vs Supply Voltage

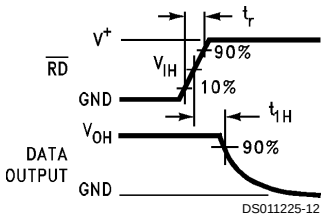


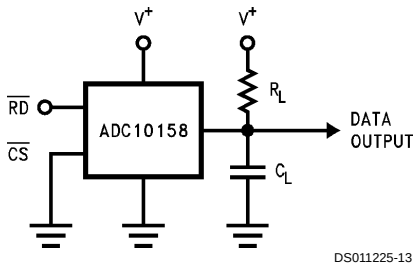
Leakage Current Test Circuit

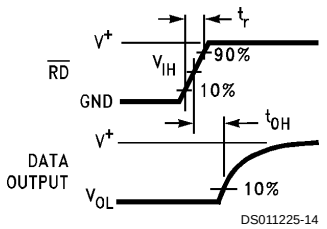


TRI-STATE Test Circuits and Waveforms









Timing Diagrams

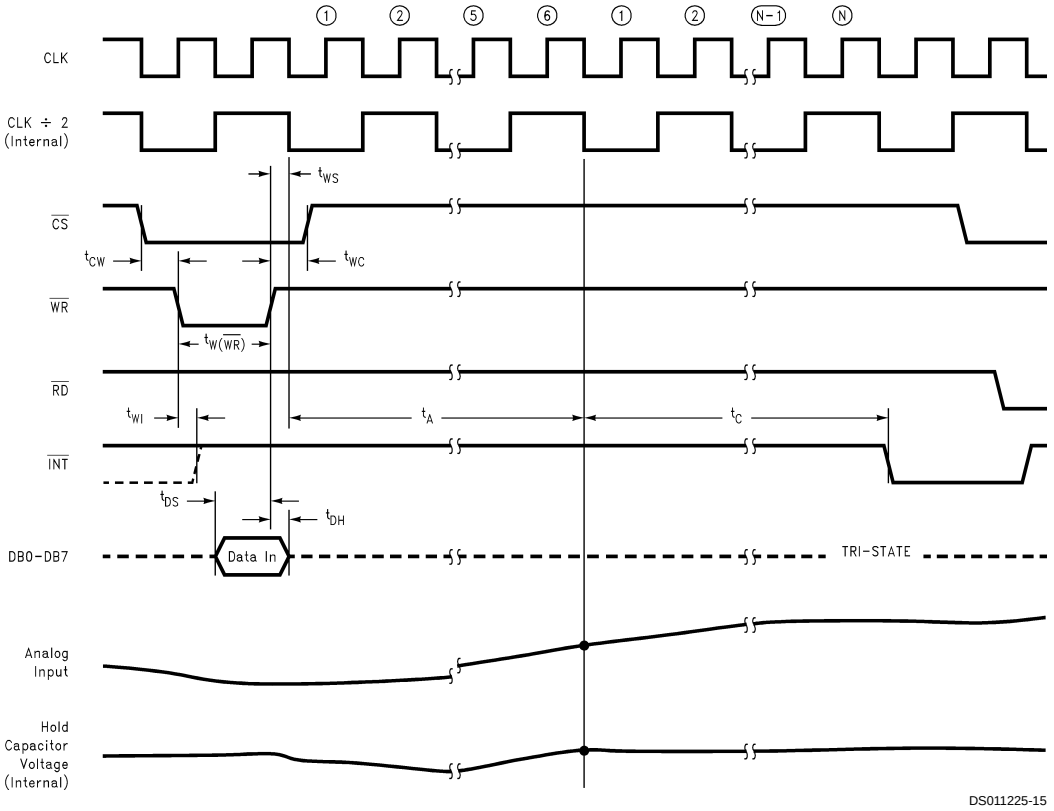


DIAGRAM 1. Starting a Conversion with New MUX Channel and Output Configuration

Timing Diagrams (Continued)

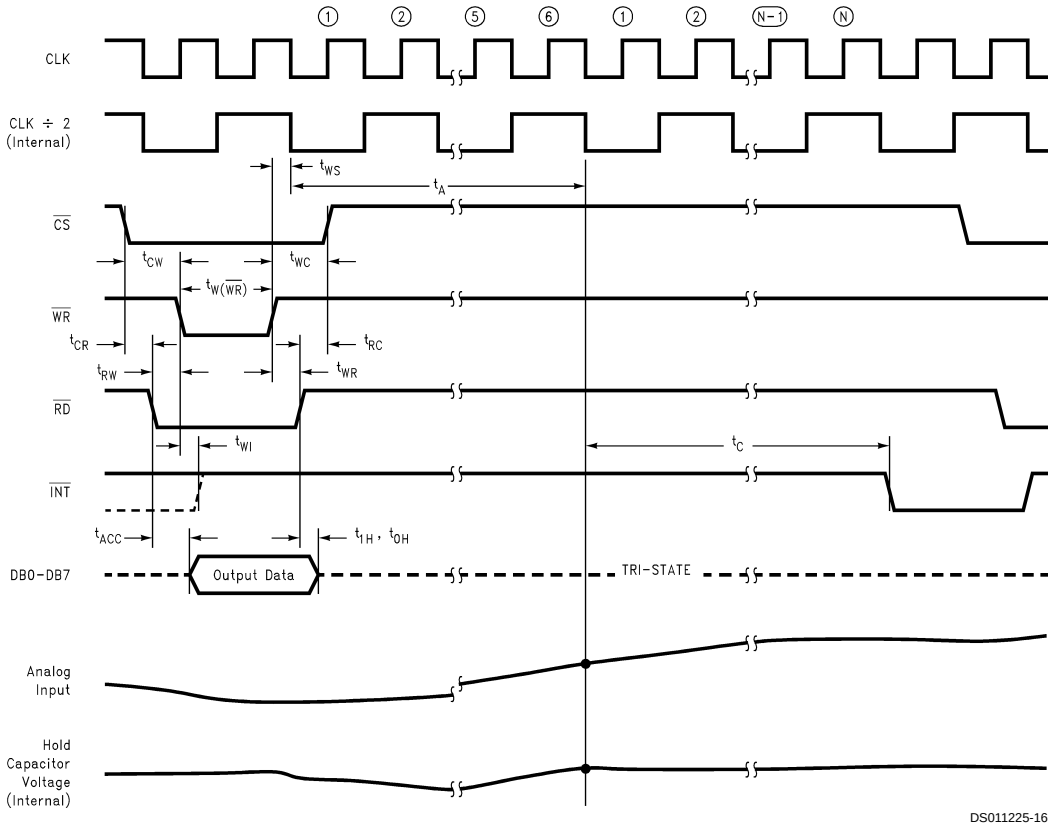


DIAGRAM 2. Starting a Conversion without Changing the MUX Channel or Output Configuration

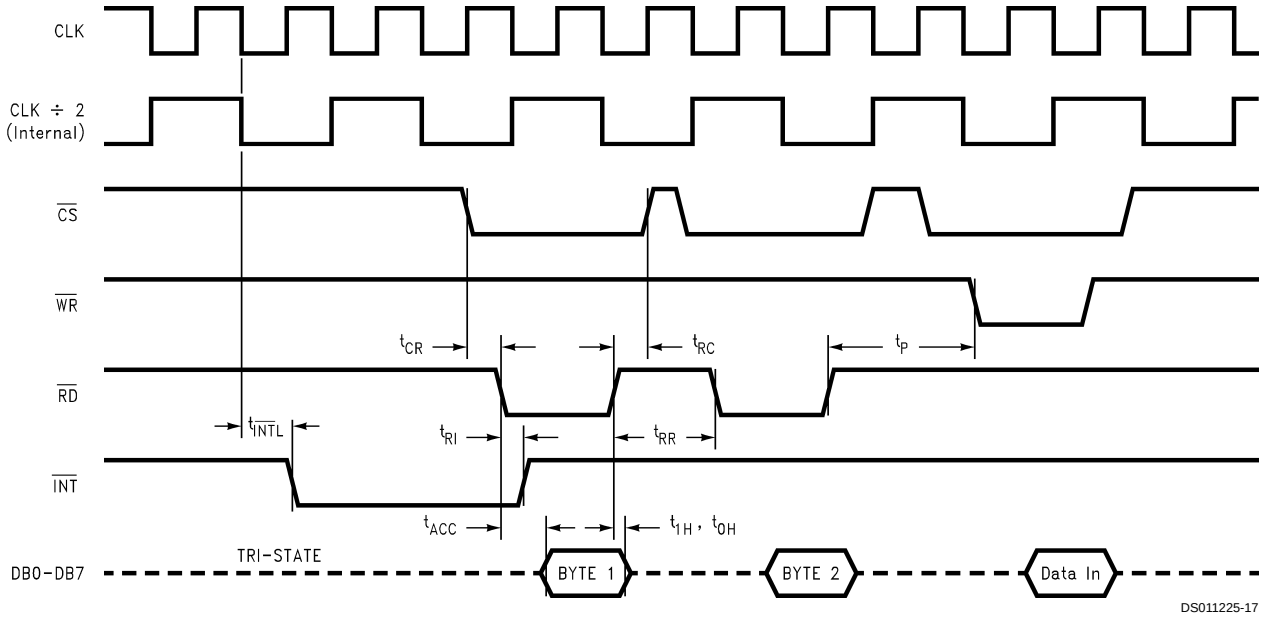


DIAGRAM 3. Reading the Conversion Result

Multiplexer Addressing and Output Data Configuration Tables

TABLE 1. ADC10154 and ADC10158 Output Data Configuration

Resolution	Output Data Format	Control Input Data			Data Bus Output Assignment								
		8/$\overline{10}$	U/$\overline{S}$	L/$\overline{R}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
10-Bits + Sign	Right-Justified	L	L	L	Sign	Sign	Sign	Sign	Sign	Sign	MSB	9	First Byte Read
					8	7	6	5	4	3	2	LSB	Second Byte Read
10-Bits + Sign	Left-Justified	L	L	H	Sign	MSB	9	8	7	6	5	4	First Byte Read
					3	2	LSB	L	L	L	L	L	Second Byte Read
10-Bits	Right-Justified	L	H	L	L	L	L	L	L	L	MSB	9	First Byte Read
					8	7	6	5	4	3	2	LSB	Second Byte Read
10-Bits	Left-Justified	L	H	H	MSB	9	8	7	6	5	4	3	First Byte Read
					2	LSB	L	L	L	L	L	L	Second Byte Read
8-Bits + Sign	Right-Justified	H	L	L	Sign	Sign	Sign	Sign	Sign	Sign	Sign	Sign	First Byte Read
					MSB	7	6	5	4	3	2	LSB	Second Byte Read
8-Bits + Sign	Left-Justified	H	L	H	Sign	MSB	7	6	5	4	3	2	First Byte Read
					LSB	L	L	L	L	L	L	L	Second Byte Read
8-Bits	Right-Justified	H	H	L	L	L	L	L	L	L	L	L	First Byte Read
					MSB	7	6	5	4	3	2	LSB	Second Byte Read
8-Bits	Left-Justified	H	H	H	MSB	7	6	5	4	3	2	LSB	First Byte Read
					L	L	L	L	L	L	L	L	Second Byte Read

TABLE 2. ADC10158 Multiplexer Addressing

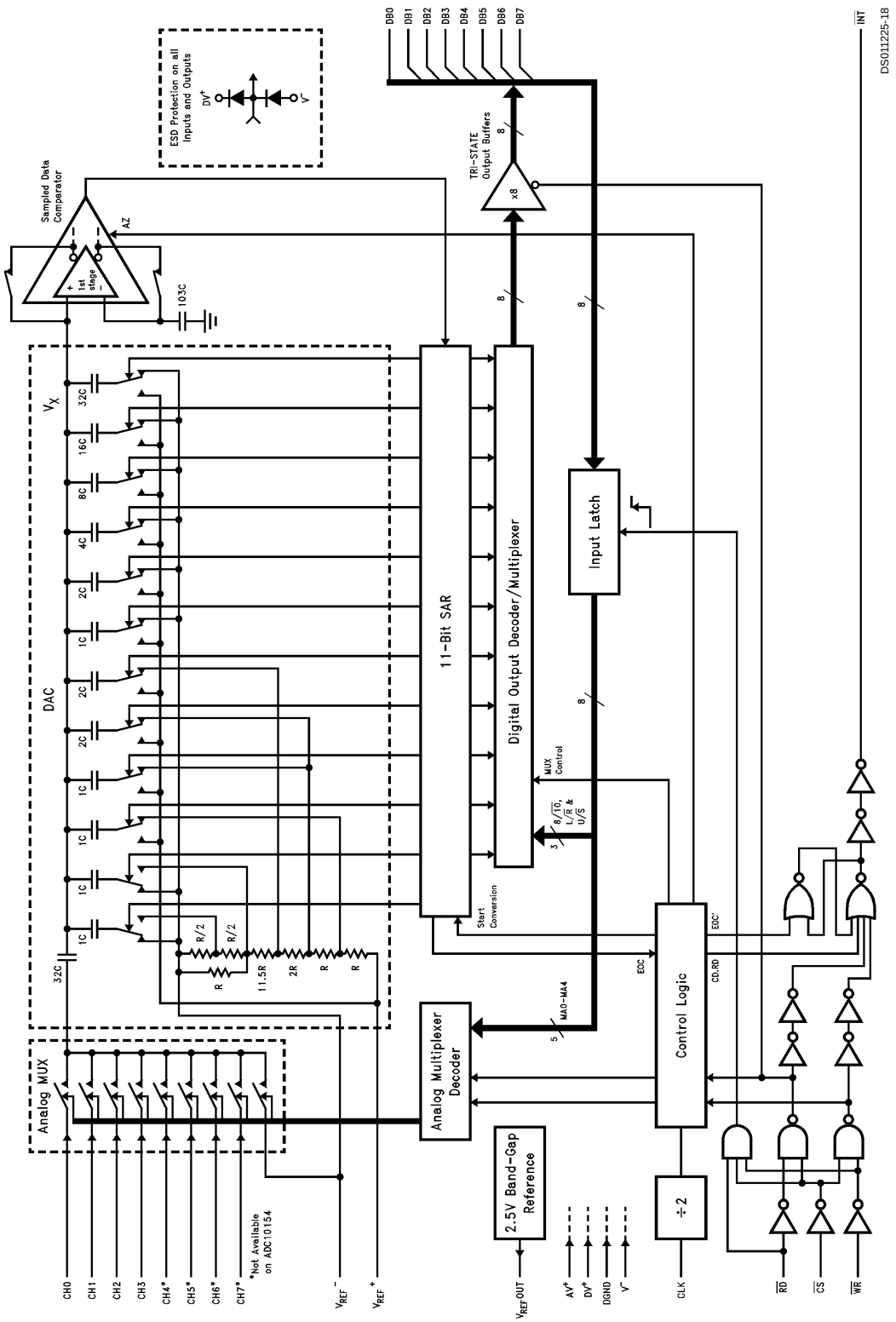
MUX Address					$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel Number									MUX Mode
MA4	MA3	MA2	MA1	MA0				CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	V_{REF}^-	
X	L	L	L	L	L		H	+	−								
X	L	L	L	H	L		H	−	+								
X	L	L	H	L	L		H			+	−						
X	L	L	H	H	L	⌐⌙	H			−	+						Differential
X	L	H	L	L	L		H					+	−				
X	L	H	L	H	L		H					−	+				
X	L	H	H	L	L		H							+	−		
X	L	H	H	H	L		H							−	+		
L	H	L	L	L	L		H	+								−	
L	H	L	L	H	L		H		+							−	
L	H	L	H	L	L		H			+						−	
L	H	L	H	H	L	⌐⌙	H				+					−	Single-Ended
L	H	H	L	L	L		H					+				−	
L	H	H	L	H	L		H						+			−	
L	H	H	H	L	L		H							+		−	
L	H	H	H	H	L		H								+	−	
H	H	L	L	L	L		H	+							−		
H	H	L	L	H	L		H		+						−		
H	H	L	H	L	L		H			+					−		
H	H	L	H	H	L	⌐⌙	H				+				−		Pseudo-Differential
H	H	H	L	L	L		H					+			−		
H	H	H	L	H	L		H						+		−		
H	H	H	H	L	L		H							+	−		
X	X	X	X	X	L	⌐⌙	L	Previous Channel Configuration									

Multiplexer Addressing and Output Data Configuration Tables (Continued)

TABLE 3. ADC10154 Multiplexer Addressing

MUX Address					$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel Number					MUX Mode
MA4	MA3	MA2	MA1	MA0				CH0	CH1	CH2	CH3	V_{REF}^-	
X	X	L	L	L	L		H	+	−				Differential
X	X	L	L	H	L	⌐⌙	H	−	+				
X	X	L	H	L	L		H			+	−		
X	X	L	H	H	L		H			−	+		
X	L	H	L	L	L		H	+				−	Single-Ended
X	L	H	L	H	L	⌐⌙	H		+			−	
X	L	H	H	L	L		H			+		−	
X	L	H	H	H	L		H				+	−	
X	H	H	L	L	L		H	+			−		Pseudo-Differential
X	H	H	L	H	L	⌐⌙	H		+		−		
X	H	H	H	L	L		H			+	−		
X	X	X	X	X	L	⌐⌙	L	Previous Channel Configuration					

Detailed Block Diagram



1.0 Functional Description

The ADC10154 and ADC10158 use successive approximation to digitize an analog input voltage. Additional logic has been incorporated in the devices to allow for the programmability of the resolution, conversion time and digital output format. A capacitive array and a resistive ladder structure are used in the DAC portion of the A/D converters. The structure of the DAC allows a very simple switching scheme to provide a very versatile analog input multiplexer. Also, inherent in this structure is a sample/hold. A 2.5V CMOS band-gap reference is also provided on the ADC10154 and ADC10158.

1.1 DIGITAL INTERFACE

The ADC10154 and ADC10158 have eight digital outputs (DB0–DB8) and can be easily interfaced to an 8-bit data bus. Taking $\overline{CS}$ and $\overline{WR}$ low simultaneously will strobe the data word on the data-bus into the input latch. This word will be decoded to determine the multiplexer channel selection, the A/D conversion resolution and the output data format. The following table shows the input word data-bit assignment.

DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
MA0	MA1	MA2	MA3	MA4	U/$\overline{S}$	8/$\overline{10}$	L/$\overline{R}$
MUX Address					Control Input Data		

DS011225-44

DB0 through DB4 are assigned to the multiplexer address data bits zero through four (MA0–MA4). *Tables 2, 3* describe the multiplexer address assignment. DB5 selects unsigned or signed (U/$\overline{S}$) operation. DB6 selects 8- or 10-bit resolution. DB7 selects left or right justification of the output data. Refer to *Table 1* for the effect the Control Input Data has on the digital output word.

The conversion process is started by the rising edge of $\overline{WR}$, which sets the "start conversion" bit inside the ADC. If this bit is set, the converter will start acquiring the input voltage on the next falling edge of the internal CLK÷2 signal. The acquisition period is 3 CLK÷2 periods, or 6 CLK periods. Immediately after the acquisition period the input signal is held and the actual conversion begins. The number of clocks required for a conversion is given in the following table:

Conversion Type	CLK÷2 Cycles	CLK Cycles (N)
8-Bit	8	16
8-Bit + Sign	9	18
10-Bit	10	20
10-Bit + Sign	11	22

Since the CLK÷2 signal is internal to the ADC, it is initially impossible to know which falling edge of CLK corresponds to the falling edge of CLK÷2. For the first conversion, the rising edge of $\overline{WR}$ should occur at least t_{WS} ns before any falling edge of CLK. If this edge happens to be on the rising edge of CLK÷2, this will add 2 CLK cycles to the total conversion time. The phase of the CLK÷2 signal can be determined at the end of the first conversion, when $\overline{INT}$ goes low. $\overline{INT}$ always goes low on the falling edge of the CLK÷2 signal. From the first falling edge of $\overline{INT}$ onward, every other falling edge of CLK will correspond to the falling edge of CLK÷2. With the phase of CLK÷2 now known, the conversion time can be minimized by taking $\overline{WR}$ high at least t_{WS} ns before the falling edge of CLK÷2.

Upon completion of the conversion, $\overline{INT}$ goes low to signal the A/D conversion result is ready to be read. Taking $\overline{CS}$ and $\overline{RD}$ low will enable the digital output buffer and put byte 1 of the conversion result on DB0 through DB7. The falling edge of $\overline{RD}$ resets the $\overline{INT}$ output high. Taking $\overline{CS}$ and $\overline{RD}$ low a second time will put byte 2 of the conversion result on DB7–DB0. *Table 1* defines the DB0–DB7 assignment for different Control Input Data. The second read does not have to be completed before a new conversion is started.

Taking $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ low simultaneously will start a conversion without changing the multiplexer channel assignment or output configuration and resolution. The timing diagram in *Figure 3* shows the sequence of events that implement this function. Refer to Diagrams 1, 2, and 3 in the Timing Diagrams section for the timing constraints that must be met.

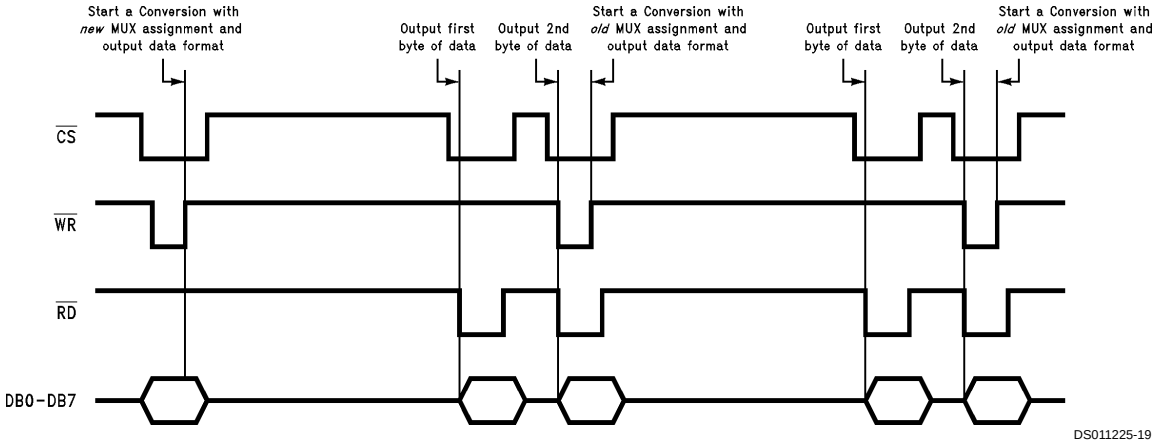


FIGURE 3. Starting a Conversion without Updating the Channel Configuration, Resolution, or Data Format

1.0 Functional Description (Continued)

Digital Interface Hints:

- Reads and writes can be completely asynchronous to CLK.
- In addition to the timing indicated in Diagrams 1–3, $\overline{CS}$ can be tied low permanently or taken low for entire conversions, eliminating all the $\overline{CS}$ guardbands (t_{CR}, t_{RC}, t_{CW}, t_{WC}).
- If $\overline{CS}$ is used as shown in Diagrams 1–-3, the $\overline{CS}$ guardbands (t_{CR}, t_{RC}, t_{CW}, t_{WC}) between $\overline{CS}$ and the $\overline{RD}$ and $\overline{WR}$ signals can safely be ignored as long as the following two conditions are met:

1) When initiating a write, $\overline{CS}$ and $\overline{WR}$ must be simultaneously low for at least $t_{W(\overline{WR})}$ ns (see Diagram 1). The "start" conversion" bit will be set on the rising edge of $\overline{WR}$ or $\overline{CS}$, whichever is first.
2) When reading data, understand that data will not be valid until t_{ACC} ns after *both* $\overline{CS}$ and $\overline{RD}$ go low. The output data will enter TRI-STATE t_{1H} ns or t_{0H} ns after *either* $\overline{CS}$ or $\overline{RD}$ goes high (see Diagrams 2 and 3).

1.2 ARCHITECTURE

Before a conversion is started, during the analog input sampling period, the sampled data comparator is zeroed. As the comparator is being zeroed the channel assigned to be the positive input is connected to the A/D's input capacitor. (See the Digital Interface section for a description of the assignment procedure.) This charges the input 32C capacitor of the DAC to the positive analog input voltage. The switches shown in the DAC portion of the detailed block diagram are set for this zeroing/acquisition period. The voltage at the input and output of the comparator are at equilibrium at this point in time. When the conversion is started the comparator feedback switches are opened and the 32C input capacitor is then switched to the assigned negative input voltage. When the comparator feedback switch opens a fixed amount of charge is trapped on the common plates of the capacitors. The voltage at the input of the comparator moves away from equilibrium when the 32C capacitor is switched to the assigned negative input voltage, causing the output of the comparator to go high ("1") or low ("0"). The SAR next goes through an algorithm, controlled by the output state of the comparator, that redistributes the charge on the capacitor array by switching the voltage on one side of the capacitors in the array. The objective of the SAR algorithm is to return the voltage at the input of the comparator as close as possible to equilibrium.

The switch position information at the completion of the successive approximation routine is a direct representation of the digital output. This information is then manipulated by the Digital Output decoder to the programmed format. The reformatted data is then available to be strobed onto the data bus (DB0–DB7) via the digital output buffers by taking $\overline{CS}$ and $\overline{RD}$ low.

2.0 Applications Information

2.1 MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sampled-data comparator structure which allows a differential analog input to be converted by the successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal or pair of input terminals being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code when configured for unsigned operation. When configured for signed operation the A/D responds with the appropriate output digital code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-ended, or pseudo-differential. *Figure 4* shows the three modes using the 4-channel MUX of the ADC10154. The eight inputs of the ADC10158 can also be configured in any of the three modes. The single-ended mode has CH0–CH3 assigned as the positive input with the negative input being the V_{REF}^- of the device. In the differential mode, the ADC10154 channel inputs are grouped in pairs, CH0 with CH1 and CH2 with CH3. The polarity assignment of each channel in the pair is interchangeable. Finally, in the pseudo-differential mode CH0–CH2 are positive inputs referred to CH3 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground-referred inputs and true differential inputs as well as signals referred to a specific voltage.

The analog input voltages for each channel can range from 50 mV below V^- (typically ground for unipolar operation or −5V for bipolar operation) to 50 mV above $V^+ = DV^+ = AV^+$ (typically 5V) without degrading conversion accuracy. If the voltage on an unselected channel exceeds these limits it may corrupt the reading of the selected channel.

2.0 Applications Information (Continued)

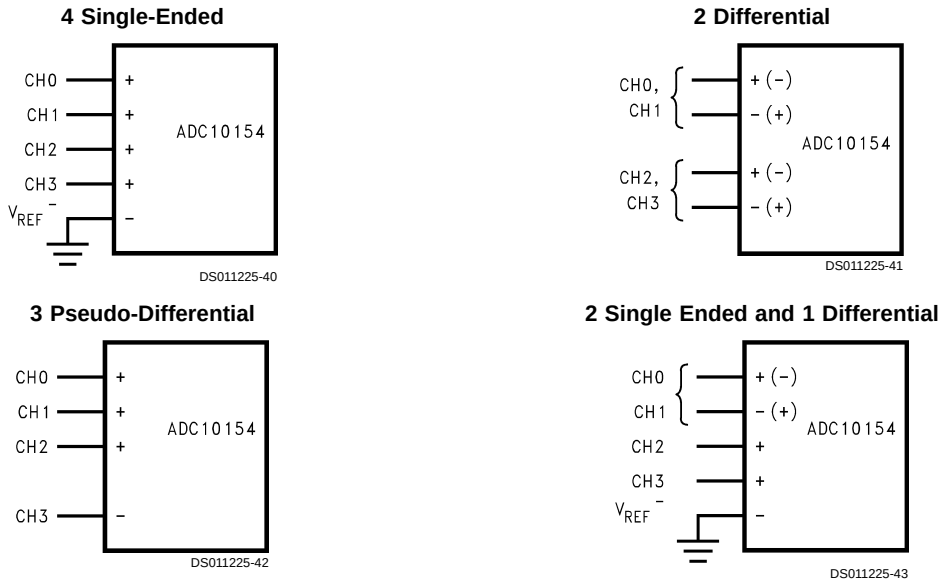


FIGURE 4. Analog Input Multiplexer Options

2.2 REFERENCE CONSIDERATIONS

The voltage difference between the V_{REF}^+ and V_{REF}^- inputs defines the analog input voltage span (the difference between V_{IN}(Max) and V_{IN}(Min)) over which the 2^n (where n is the programmed resolution) possible output codes apply. In the pseudo-differential and differential modes the actual voltage applied to V_{REF}^+ and V_{REF}^- can lie anywhere between the AV^+ and V^-. Only the difference voltage is of importance. When using the single-ended multiplexer mode the voltage at V_{REF}^- has a dual function. It simultaneously determines the "zero" reference voltage and, with V_{REF}^+, the analog voltage span.

The value of the voltage on the V_{REF}^+ or V_{REF}^- inputs can be anywhere between AV^+ + 50 mV and V^- − 50 mV, so long as V_{REF}^+ is greater than V_{REF}^-. The ADC10154 and ADC10158 can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the minimum reference input resistance of 4.5 kΩ.

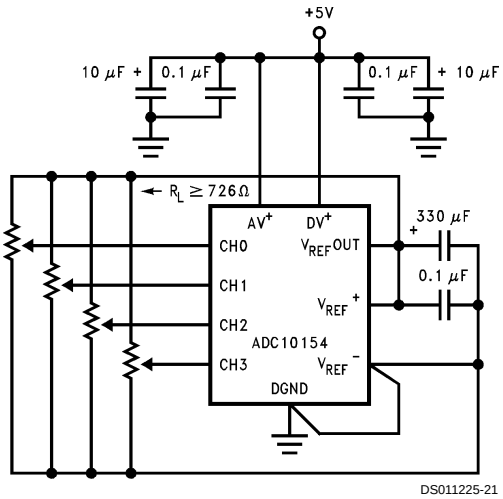
The internal 2.5V bandgap reference in the ADC10154 and ADC10158 is available as an output on the VREFOut pin. To ensure optimum performance this output needs to be bypassed to ground with 330 µF aluminum electrolytic or tantalum capacitor. The reference output is unstable with capacitive loads greater than 100 pF and less than 100 µF. Any capacitive loads ≤100 pF or ≥100 µF will not cause the reference to oscillate. Lower output noise can be obtained by increasing the output capacitance. The 330 µF capacitor will yield a typical noise floor of 200 nVrms/$\sqrt{Hz}$.

The 2.5V reference output is referred to the negative supply pin (V^-). Therefore, **the voltage at VREFOut will always be 2.5V greater than the voltage applied to V^-.** Applying this voltage to V_{REF}^+ with V_{REF}^- tied to V^- will yield an analog voltage span of 2.5V. In bipolar operation the voltage at VREFOut will be at −2.5V when V^- is tied to −5V. For the single-ended multiplexer mode the analog input voltage range will be from −5V to −2.5V. The pseudo-differential and differential multiplexer modes allow for more flexibility in the analog input voltage range since the "zero" reference voltage is set by the actual voltage applied to the assigned negative input pin. The drawback of using the internal reference in the bipolar mode is that any noise on the −5V tied to the V^- pin will affect the conversion result. The bandgap reference is specified and tested in unipolar operation with V^- tied to the system ground.

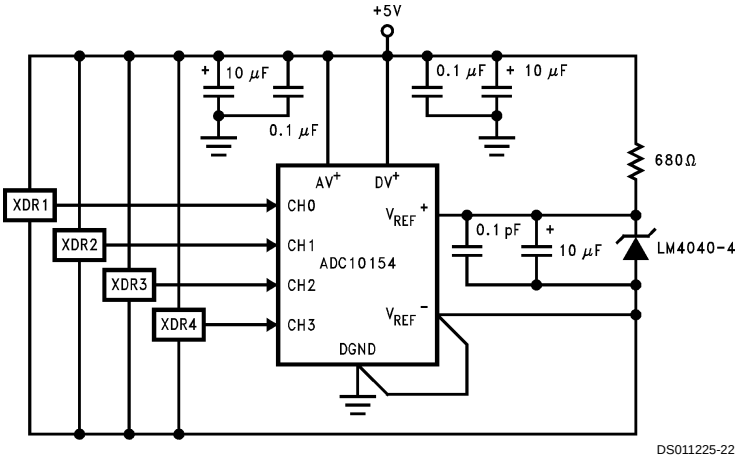
In a ratiometric system (*Figure 5* **(a)**), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage may also be the system power supply, so V_{REF}^+ can also be tied to AV^+. This technique relaxes the stablity requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 5* **(b)**), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time- and temperature-stable voltage source that has excellent initial accuracy. The LM4040 and LM185 references are suitable for use with the ADC10154 and ADC10158.

2.0 Applications Information (Continued)



a. Ratiometric Using the Internal Reference



b. Absolute Using a 4.096V Span

FIGURE 5. Different Reference Configurations

The minimum value of V_{REF} ($V_{REF} = V_{REF}^{+} - V_{REF}^{-}$) can be quite small (see Typical Performance Characteristics) to allow direct conversion of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/2^n$).

2.3 THE ANALOG INPUTS

Due to the sampling nature of the analog inputs, at the clock edges short duration spikes of current will be seen on the selected assigned negative input. Input bypass capacitors should not be used if the source resistance is greater than 1 kΩ since they will average the AC current and cause an effective DC current to flow through the analog input source resistance. An op amp RC active lowpass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required. Bypass capacitors may be used when the source impedance is very low without any degradation in performance.

In a true differential input stage, a signal that is common to both "+" and "−" inputs is cancelled. For the ADC10154 and ADC10158, the positive input of a selected channel pair is only sampled once before the start of a conversion during the acquisition time (t_A). The negative input needs to be stable during the complete conversion sequence because it is sampled before each decision in the SAR sequence. Therefore, any AC common-mode signal present on the analog inputs will not be completely cancelled and will cause some conversion errors. For a sinusoid common-mode signal this error is:

$V_{error}(Max) = V_{PEAK}\ (2\pi f_{CM})(t_C)$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value, and t_C is the A/D's maximum conversion time ($t_C = 22/f_{CLK}$ for 10-bit plus sign resolution). For example, for a 60 Hz common-mode signal to generate a ¼ LSB error (1.24 mV) with a 4.5 µs conversion time, its peak value would have to be approximately 731 mV.

2.4 OPTIONAL ADJUSTMENTS

2.4.1 Zero Error

The zero error of the A/D converter relates to the location of the first riser of the transfer function (see *Figure 1*) and can be measured by grounding the minus input and applying a small magnitude positive or negative voltage to the plus input. Zero error is the difference between actual DC input

2.0 Applications Information

(Continued)

voltage which is necessary to just cause an output digital code transition from 000 0000 0000 to 000 0000 0001 (10-bits plus sign) and the ideal ½ LSB value (½ LSB = 2.44 mV for V_{REF} = + 5.000V and 10-bit plus sign resolution).

The zero error of the A/D does not require adjustment. If the minimum analog input voltage value, V_{IN}(Min), is not ground, the effetive "zero" voltage can be adjusted to a convenient value. The converter can be made to output an all zeros digital code for this minimum input voltage by biasing any minus input to V_{IN}(Min). This is useful for either the differential or pseudo-differential input channel configurations.

2.4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the V_{REF} voltage ($V_{REF} = V_{REF}^{+} - V_{REF}^{-}$) for a digital output code changing from 011 1111 1110 to 011 1111 1111. In bipolar signed operation this only adjusts the positive full scale error. The negative full-scale error will be as specified in the Electrical Characteristics after a positive full-scale adjustment.

2.4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A plus input voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/2^n, n being the programmed resolution) is applied to selected plus input and the zero reference voltage at the corresponding minus input should then be adjusted to just obtain the 000_{HEX} to 001_{HEX} code transition.

The full-scale adjustment should be made [with the proper minus input voltage applied] by forcing a voltage to the plus input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{2^n}\right]$$

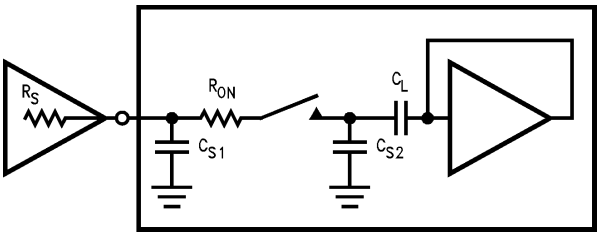
where V_{MAX} equals the high end of the ananlog input range, V_{MIN} equals the low end (the offset zero) of the analog range and n equals the programmed resolution. Both V_{MAX} and V_{MIN} are ground referred. The V_{REF} ($V_{REF} = V_{REF}^{+} - V_{REF}^{-}$) voltage is then adjusted to provide a code change from $3FE_{HEX}$ to $3FF_{HEX}$. Note, when using a pseudo-differential or differential multiplexer mode where V_{REF}^{+} and $V_{REF}-$ are placed within the V^{+} and V^{-} range, the individual values of V_{REF}^{+} and V_{REF}^{-} do not matter, only the difference sets the analog input voltage span. This completes the adjustment procedure.

2.5 INPUT SAMPLE-AND-HOLD

The ADC10154/8's sample/hold capacitor is implemented in the capacitor array. After the channel address is loaded, the array is switched to sample the selected positive analog input. The rising edge of $\overline{WR}$ loads the multiplexer addressing information. The sampling period for the assigned positive input is maintained for the duration of the acquisition time (t_A), i.e., approximately 6 to 8 clock cycles after the rising edge of $\overline{WR}$.

An acquisition window of 6 clock cycles is available to allow the voltage on the capacitor array to settle to the positive analog input voltage. Any change in the analog voltage on a selected positive input before or after the acquisition window will not effect the A/D conversion result.

In the simplest case, the array's acquisition time is determined by the R_{ON} (9 kΩ) of the multiplexer switches, the stray input capacitance C_{S1} (3.5 pF) and the total array (C_L) and stray (C_{S2}) capacitance ($C_L + C_{S2}$ = 48 pF). For a large source resistance the analog input can be modeled as an RC network as shown in *Figure 6*. The values shown yield an acquisition time of about 1.1 µs for 10-bit unipolar or 10-bit plus sign bipolar accuracy with a zero-to-full-scale change in the input voltage. External source resistance and capacitance will lengthen the acquisition time and should be accounted for. Slowing the clock will lengthen the acquisition time, thereby allowing a larger external source resistance.



DS011225-23

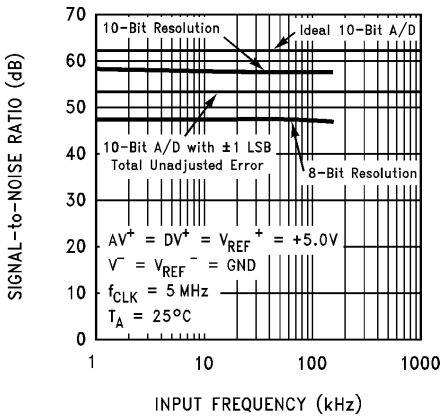
FIGURE 6. Analog Input Model

The curve "Signal to Noise Ratio vs. Output Frequency" (*Figure 7*) gives an indication of the usable bandwidth of the ADC10154/ADC10158. The signal-to-noise ratio of an ideal A/D is the ratio of the RMS value of the full scale input signal amplitude to the value of the total error amplitude (including noise) caused by the transfer function of the A/D. An ideal 10-bit plus sign A/D converter with a total unadjusted error of 0 LSB would have a signal-to-noise ratio of about 68 dB, which can be derived from the equation:

$$S/N = 6.02(n) + 1.76$$

where S/N is in dB and n is the number of bits. *Figure 3* shows the signal-to-noise ratio vs. input frequency of a typical ADC10154/ADC10158 with ½ LSB total unadjusted error. The dotted lines show signal-to-noise ratios for an ideal (noiseless) 10-bit A/D with 0 LSB error and an A/D with a 1 LSB error.

SNR vs Input Frequency



DS011225-24

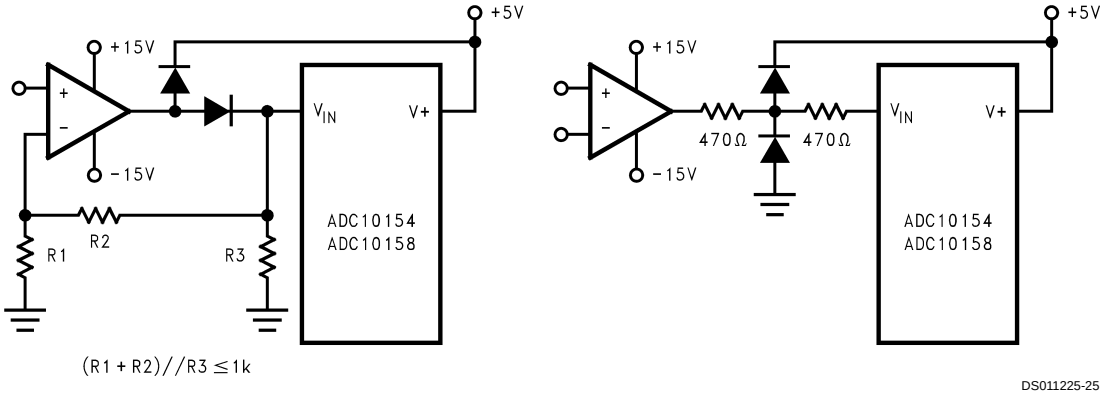
FIGURE 7. ADC10154/ADC10158 Signal-to-Noise Ratio vs Input Frequency

2.0 Applications Information

(Continued)

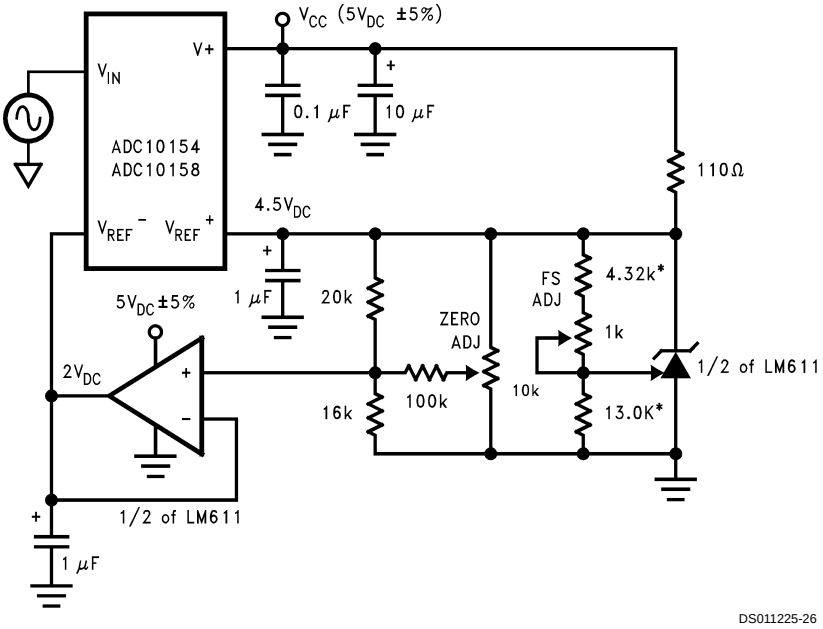
The sample-and-hold error specifications are included in the error and timing specifications of the A/D. The hold step and gain error sample/hold specs are included in the ADC10154/ADC10158's total unadjusted, linearity, gain and offset error specifications, while the hold settling time is included in the A/D's maximum conversion time specification. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. The data is lost after a new conversion has been completed.

Protecting the Analog Inputs



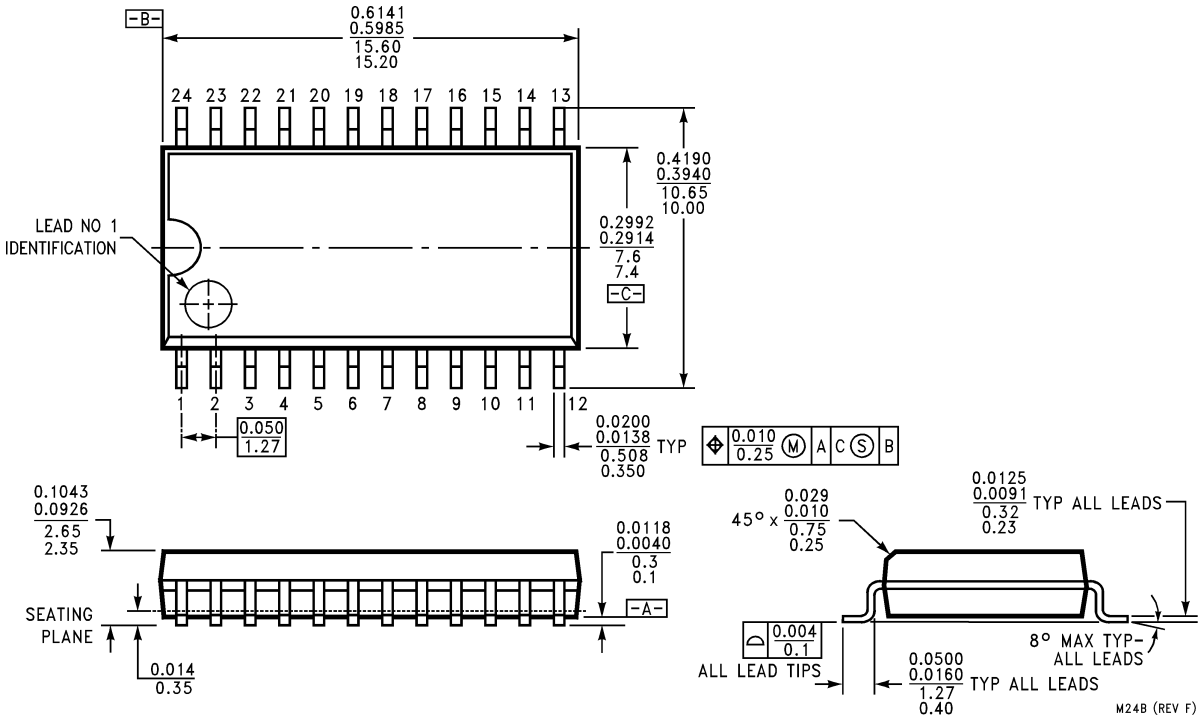
Diodes are 1N914.
The protection diodes should be able to withstand the output current of the op amp under current limit.

Zero-Shift and Span-Adjust for Signed or Unsigned, Unipolar, Single-Ended Multiplexer Assignment, Analog Input Range of 2V ≤ V_{IN} ≤ 4.5V

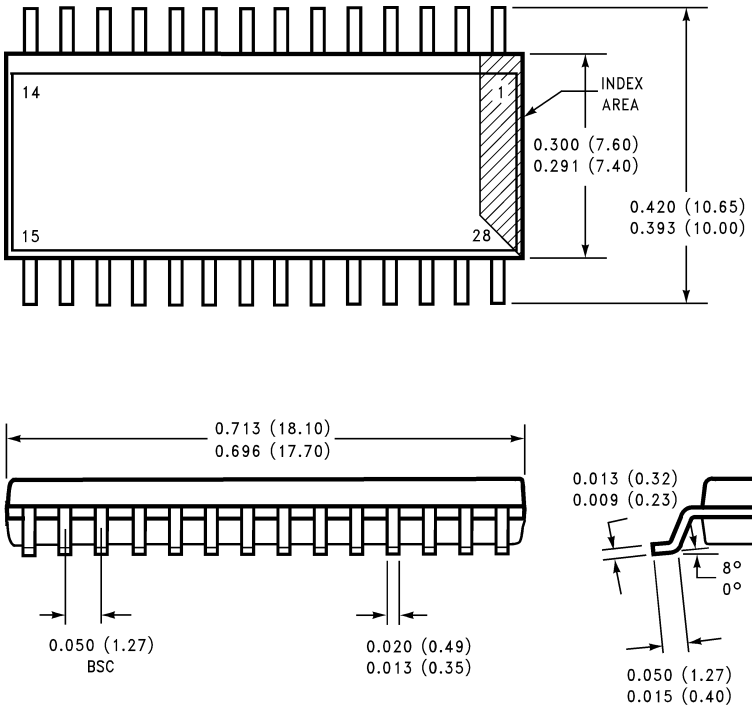


*1% resistors

Physical Dimensions inches (millimeters) unless otherwise noted

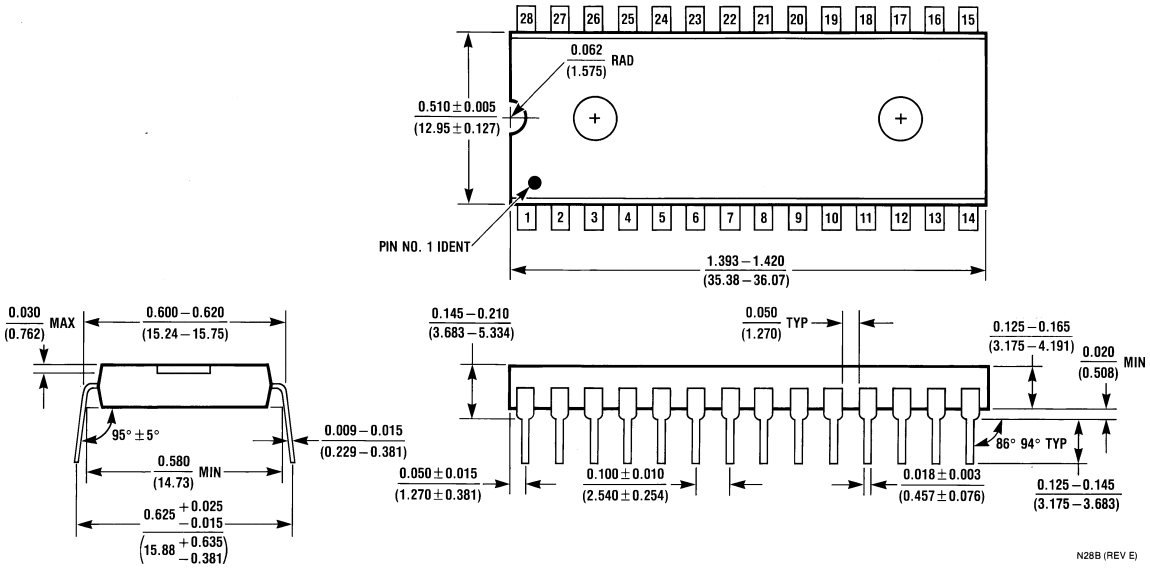


Dual-In-Line Package (M)
Order Number ADC10154CIWM
NS Package Number M24B



Dual-In-Line Package (M)
Order Number ADC10158CIWM
NS Package Number M28B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number ADC10158BIN or ADC10158CIN
NS Package Number N28B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.